ECE 3120 Computer Systems Instructions

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The LOAD and STORE Instructions

- The LOAD instruction copies the contents of a memory location or places an immediate value into an accumulator or a CPU register.
- STORE instructions save the contents of a CPU register into a memory location.
- N and Z flags of the CCR register are automatically updated and the V flag is cleared.
- All except for the relative mode can be used to select the memory location or value to be loaded into an accumulator or CPU register.
- All except for the relative and immediate modes can be used to select memory location to store contents of the CPU register. For example,

ldaa 0,X

staa \$20

stx \$8000

ldd #100

Table 1.4 Load and store instructions

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Mnemonic	Function	Operation		
LDAA LDAB LDD LDS LDX LDY LEAS LEAX	Load A Load B Load D Load SP Load index register X Load index register Y Load effective address into SP Load effective address into X	$(M) \Rightarrow A$ $(M) \Rightarrow B$ $(M:M+1) \Rightarrow (A:B)$ $(M:M+1) \Rightarrow SP$ $(M:M+1) \Rightarrow X$ $(M:M+1) \Rightarrow X$ Effective address $\Rightarrow SP$ Effective address $\Rightarrow X$		
LEAY	Load efective address into Y	Effective address $\Rightarrow Y$		
Store Instructions				
Mnemonic	Function	Operation		
STAA STAB STD STS STX STY	Store A Store B Store D Store SP Store X Store Y	$(A) \Rightarrow M$ $(B) \Rightarrow M$ $(A) \Rightarrow M, (B) \Rightarrow M+1$ $(SP) \Rightarrow M, M+1$ $(X) \Rightarrow M:M+1$ $(Y) \Rightarrow M:M+1$		

Transfer and Exchange Instructions

- Transfer instructions copy the contents of a CPU register or accumulator into another CPU register or accumulator.
- TFR is the universal transfer instruction, but other mnemonics are accepted for compatibility with the 68HC11.
- The TAB and TBA instructions affect the N, Z, and V condition code bits.
- The TFR instruction does not affect any condition code bits. For example,

TFR D,X ; [D] \Rightarrow X

TFR A,B $; [A] \Rightarrow B$

- The EXG instruction exchanges the contents of a pair of registers or accumulators. For example,

exg A, B

exg D,X

- The SEX instruction sign-extend an 8-bit two's complement number into a 16-bit number so that it can be used in 16-bit signed operations. For example,

SEX A,X

Move Instructions

- These instructions move data bytes or words from a source to a destination in memory.
- Six combinations of immediate, extended, and index addressing modes are allowed to specify the source and destination addresses:

 $IMM \Rightarrow EXT$, $IMM \Rightarrow IDX$, $EXT \Rightarrow EXT$,

 $EXT \Rightarrow IDX$, $IDX \Rightarrow EXT$, $IDX \Rightarrow IDX$

- Examples:

movb \$100,\$800

movw 0,X, 0,Y

Table 1.6 Move instructions				
Transfer Instructions				
Mnemonic	Function	Operation		
MOVB MOVW	Move byte (8-bit) Move word (16-bit)	$(M1) \Rightarrow M2$ $(M:M+1_1) \Rightarrow M:M+1_2$		

Add and Subtract Instructions

- These instructions perform fundamental arithmetic operations.
- The destinations of these instructions are always a CPU register or accumulator.

- For example,

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adda $800 ; A \leftarrow [A] + [\$800]
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adca
$$\$800$$
 ; $A \Leftarrow [A] + [\$800] + C$

suba
$$\$802$$
 ; $A \Leftarrow [A] + [\$802]$

sbca
$$\$800$$
 ; A \Leftarrow [A] - [$\$800$] - C

Table 1.7 Add and subtract instructions

Add Instructions			
Mnemonic	Function	Operation	
ABA ABX ABY ADCA ADCB ADDA ADDB ADDD	Add B to A Add B to X Add B to Y Add with carry to A Add with carry to B Add without carry to B Add without carry to B Add without carry to B	$(A) + (B) \Rightarrow A$ $(B) + (X) \Rightarrow X$ $(B) + (Y) \Rightarrow Y$ $(A) + (M) + C \Rightarrow A$ $(B) + (M) + C \Rightarrow B$ $(A) + (M) \Rightarrow A$ $(B) + (M) \Rightarrow B$ $(A:B) + (M:M+1) \Rightarrow A:B$	
Subtract Instructions			
Mnemonic	Function	Operation	
SBA SBCA SBCB SUBA SUBB SUBD	Subtract B from A Subtract with borrow from A Subtract with borrow from B Subtract memory from A Subtract memory from B Subtract memory from D	$(A) - (B) \Rightarrow A$ $(A) - (M) - C \Rightarrow A$ $(B) - (M) - C \Rightarrow B$ $(A) - (M) \Rightarrow A$ $(B) - (M) \Rightarrow B$ $(D) - (M:M+1) \Rightarrow D$	