ECE3120: Computer Systems
Chapter 7: Parallel Ports

Manjeera Jeedigunta
http://blogs.cae.tntech.edu/msjeedigun21
Email: msjeedigun21@tntech.edu
Tel: 931-372-6181, Prescott Hall 120

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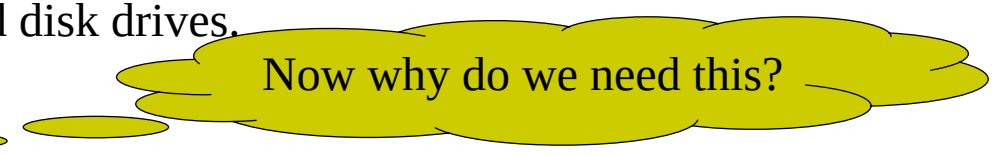
Basic Concepts of I/O

- I/O devices are also called peripheral devices.
- I/O devices are pieces of equipment that exchange data with a computer. Examples include switches, light-emitting diodes, cathode-ray tube screens, printers, modems, keyboards, and disk drives.



Interface (peripheral) chip

- A chip whose function is to synchronize data transfer between the CPU and I/O devices.
- An interface may consist of **control registers**, **status registers**, **data direction registers**, **data registers**, and **control circuitry**.
- An interface chip has **data pins** that are connected to the CPU and **I/O port pins** that are connected to the I/O devices.
- Each interface chip has a chip enable signal input or inputs which, when asserted, allow the interface chip to react to the data transfer request.
- Data transfer between an I/O device and the CPU can be proceeded **bit-by-bit** (serial) or in **multiple bits** (parallel).

- Address decoder makes sure that each time one and only one peripheral device respond to the CPU's I/O request.

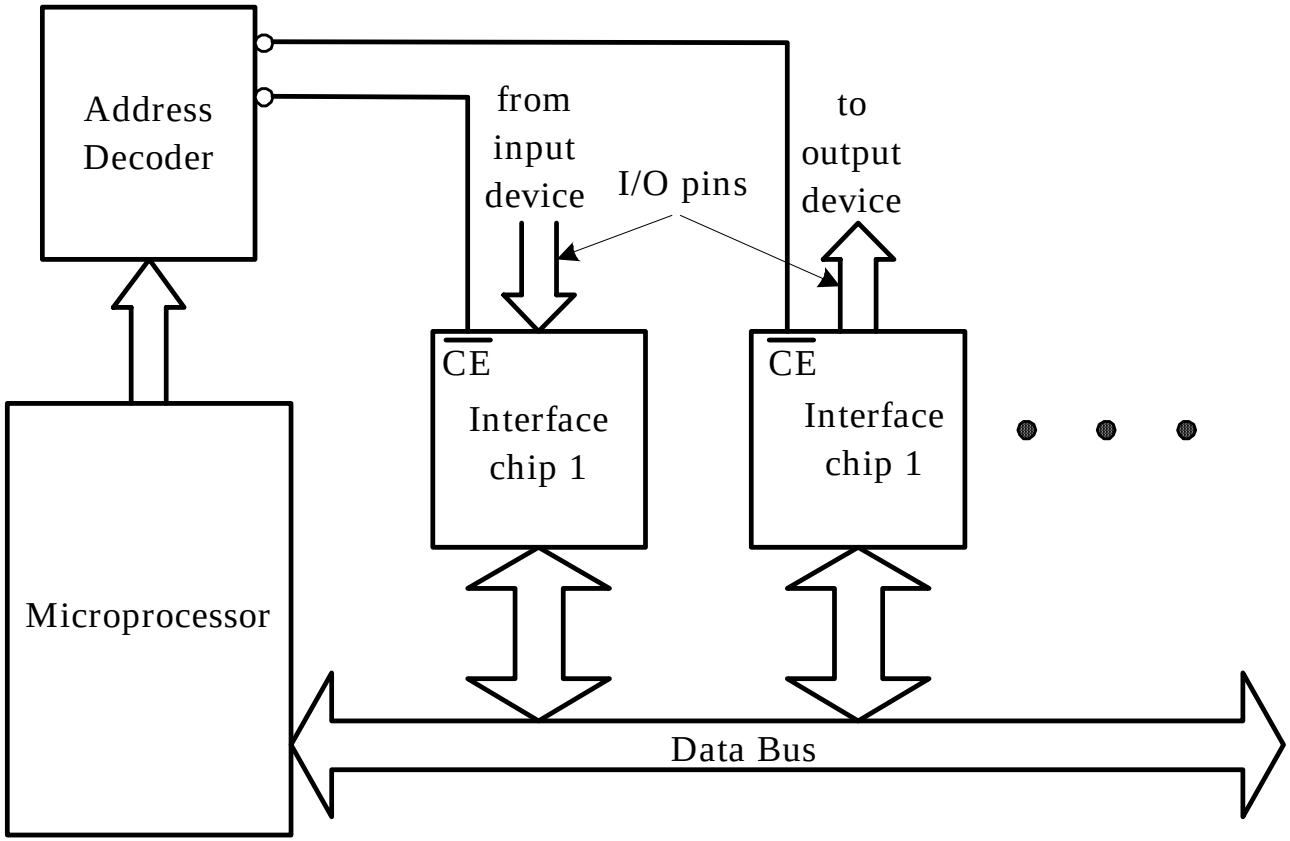


Figure 7.1 Interface chip, I/O devices, and microprocessor

I/O Addressing

1. Isolated I/O scheme

- The microprocessor has dedicated instructions for I/O operations.
- The microprocessor has a separate address space for I/O devices.

2. Memory-mapped I/O scheme

- The microprocessor uses the same instruction set to perform memory accesses and I/O operations.
- The I/O devices and memory components are resident in the same memory space.

I/O Transfer Synchronization

The role of an interface chip

1. Synchronizing data transfer between the CPU and the interface chip.
2. Synchronizing data transfer between the interface chip and the I/O device.

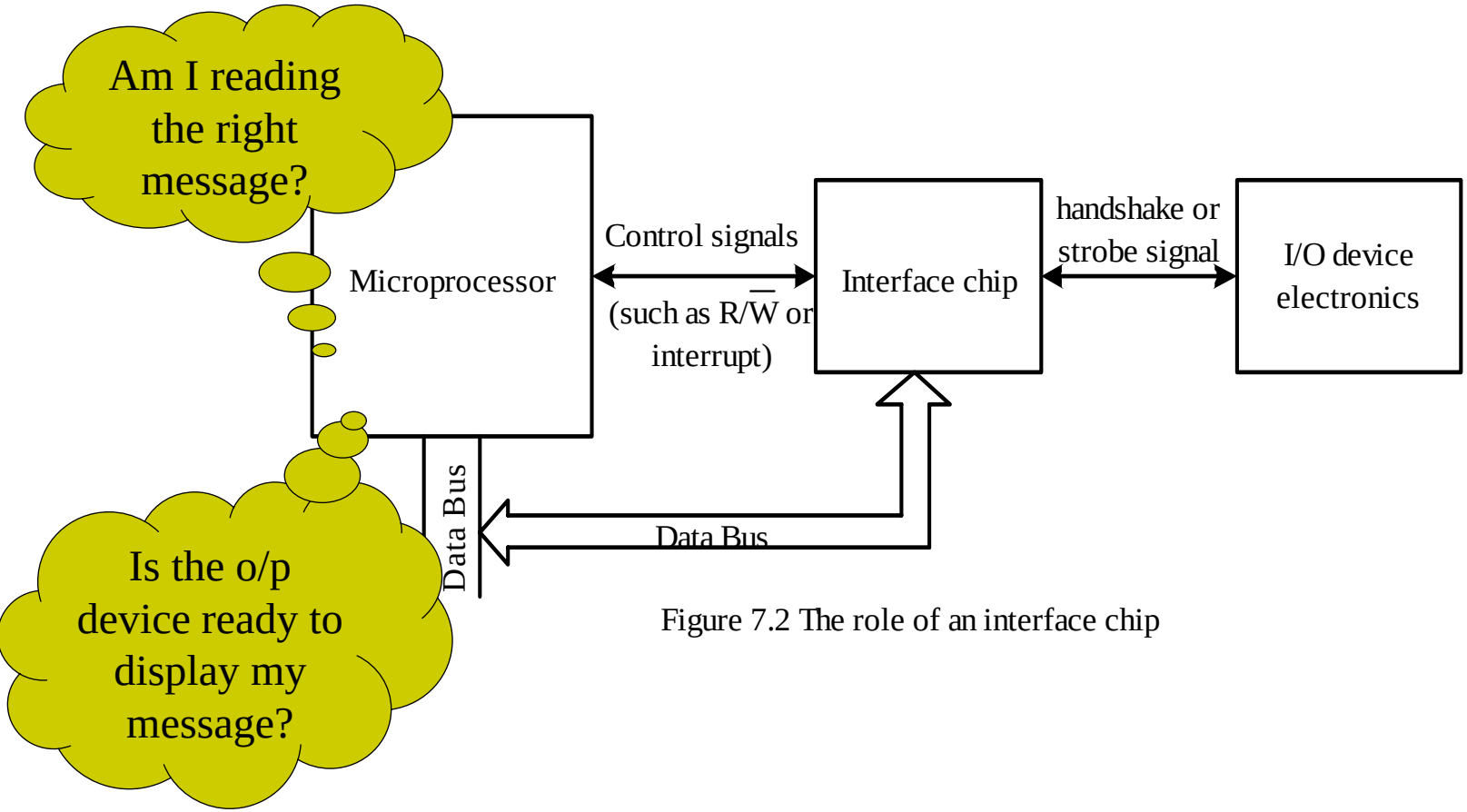


Figure 7.2 The role of an interface chip

Synchronizing the Microprocessor and the Interface Chip

The polling method

1. For input -- the microprocessor checks a status bit of the interface chip to find out if the interface chip has received new data from the input device.
2. For output -- the microprocessor checks a status bit of the interface chip to find out if it can send new data to the interface chip.

The interrupt-driven method

1. For input -- the interface chip interrupts the microprocessor whenever it has received new data from the input device.
2. For output -- the interface chip interrupts the microprocessor whenever it can accept new data from the microprocessor.

Synchronizing the Interface Chip and the I/O Devices

- ***Brute-force method***

- ***The strobe method***

- ***The handshake method***.

Synchronizing the Interface Chip and the I/O Devices

Brute-force method -- nothing special is done.

- Useful when the data timing is unimportant, supported by all I/O ports of 68HCS12.

1. For input -- The microprocessor reads the interface chip and the interface chip returns the voltage levels on the input port pins to the microprocessor.

2. For output -- The interface chip places the data that it received from the microprocessor directly on the output port pins.

Synchronizing the Interface Chip and the I/O Devices

The strobe method -- a strobe signal is used to indicate that data are stable on I/O port pins, useful when the chip and I/O device can keep up with each other.

- Not supported by 68HCS12 parallel ports.

1. For input -- the interface chip latches the data into its data register using the strobe signal.

2. For output -- the interface chip places the data on port pins that it received from the microprocessor and asserts the strobe signal. The output device latches the data using the strobe signal.

Synchronizing the Interface Chip and the I/O Devices

The handshake method -- used when timing is crucial, not supported by 68HCS12 parallel ports.

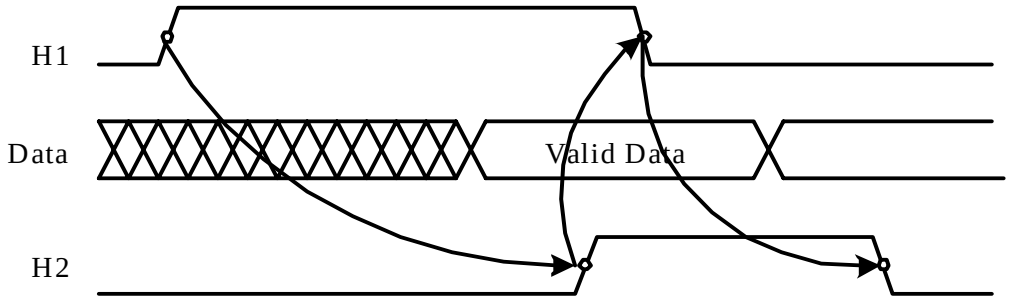
-Two handshake signals are used to synchronize the data transfer. One signal, call it H1, is asserted by the interface chip. The other signal, call it H2, is asserted by the I/O device.

-Two handshake modes are available –

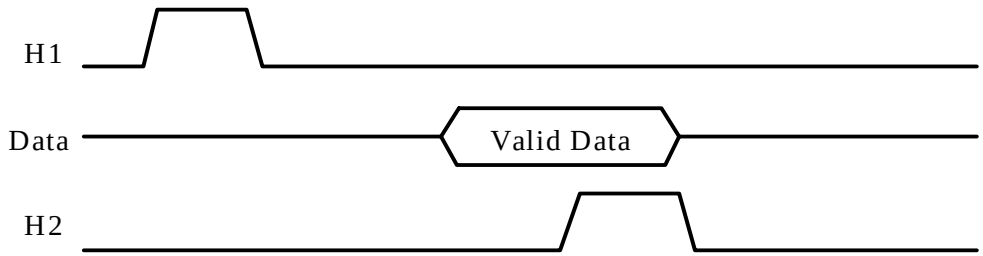
- -pulse mode
- -interlocked mode.

Input Handshake Protocol

Step 1. The interface chip asserts (or pulses) H1 to indicate its intention to input data.
Step 2. The input device puts data on the data port pins and also asserts (or pulses) the handshake signal H2.
Step 3. The interface chip latches the data and de-asserts H1. After some delay, the input device also de-asserts H2.



(a) Interlocked



(b) Pulse mode

Figure 7.3 Input Handshakes

Output Handshake Protocol

Step 1. The interface chip places data on the port pins and asserts (or pulses) H1 to indicate that it has valid data to be output.

Step 2. The output device latches the data and asserts (or pulses) H2 to acknowledge the receipt of data.

Step 3. The interface chip de-asserts H1 following the assertion of H2. The output device then de-asserts H2.

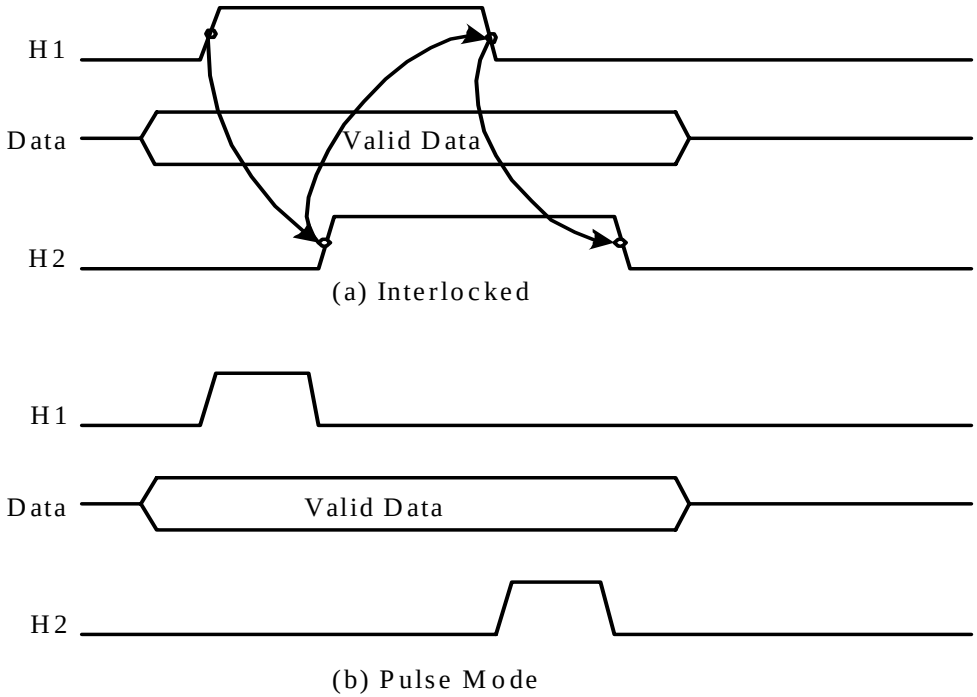


Figure 7.4 Output Handshaking