ECE3120: Computer Systems
Chapter 8: Timer Module

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Why are Timer Functions Important?

- It is very difficult and impossible to implement the following applications without a timer function:
  - Period and pulse width measurement
  - Frequency measurement
  - Event counting
  - Arrival time comparison
  - Time-of-day tracking
  - Periodic interrupt generation
  - Waveform generation

The HCS12 Timer System (1 of 2)

- The HCS12 has a standard timer module (TIM) that consists of:
  - Eight channels of multiplexed input capture and output compare functions.
  - 16-bit pulse accumulator A
  - 16-bit timer counter
  - The TIM block diagram is shown in Figure 8.1.

- The TIM shares the eight Port T pins (IOC0…IOC7).

The HCS12 Timer System (2 of 2)

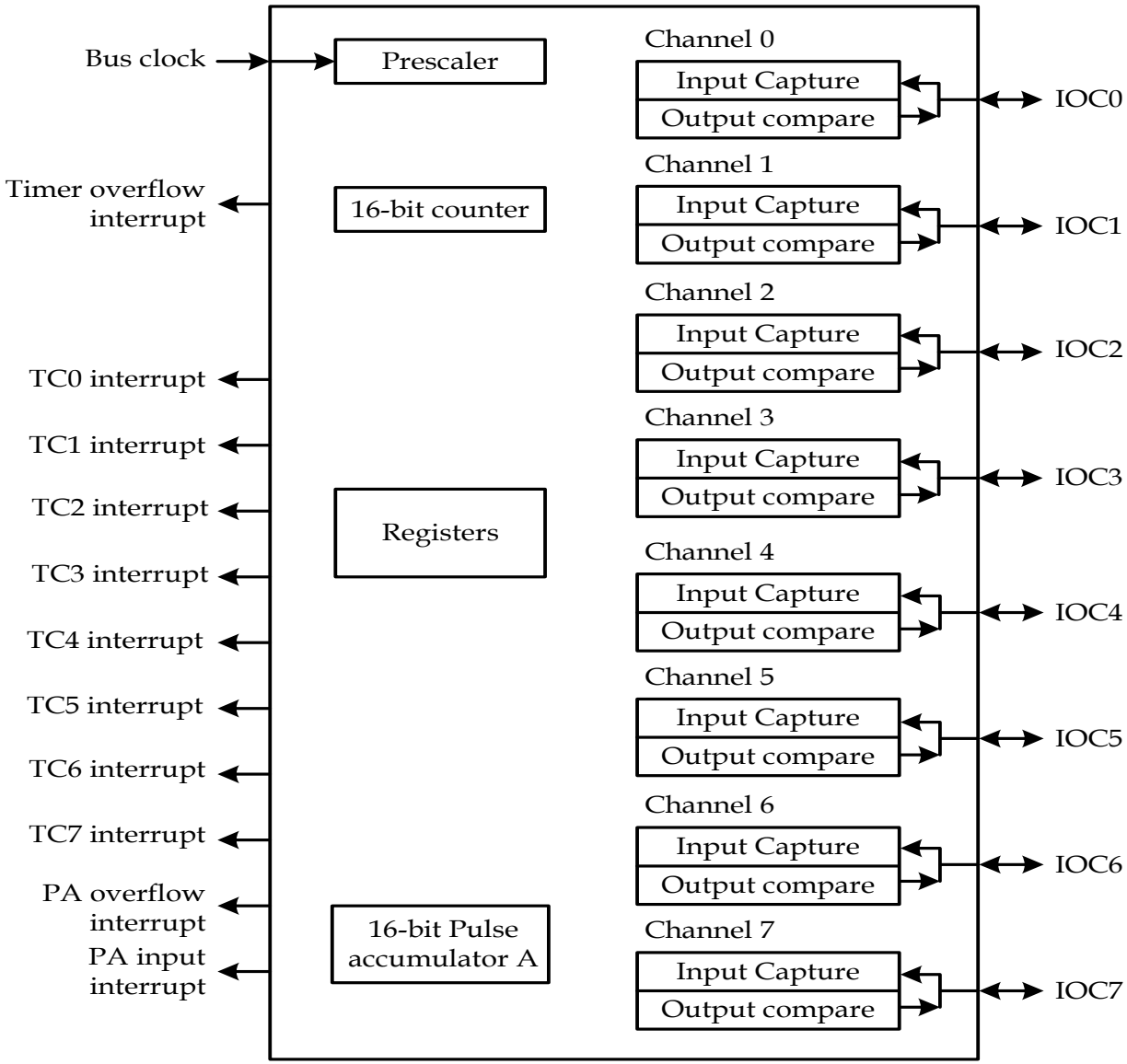

Figure 8.1 HCS12 Standard Timer (TIM) block diagram

Important Timer Functions

- Input Capture
  - Pulse Width Measurement
  - Period Measurement
  - Duty Cycle
  - Event arrival time recording
  - Time reference
- Output Compare
  - Triggers an action on a pin (set to high, low, toggle)
  - Sets a flag in a register
  - Generates an interrupt request

Timer Counter Register (TCNT)

- Required for input capture and output compare functions
- Must be accessed in one 16-bit operation in order to obtain the correct value
- Three other registers related to the operation of the TCNT: TSCR1, TSCR2, TFLG2.

Timer System Control Register 1 (TSCR1)

- The contents of TSCR1 are shown in Figure 8.2.
- Setting and clearing the bit 7 of TSCR1 will start and stop the counting of the TCNT.
- Setting the bit 4 will enable fast timer flag clear function. If this bit is clear, then the user must write a one to a timer flag in order to clear it.

	7	6	5	4	3	2	1	0
	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
value after reset	0	0	0	0	0	0	0	0

TEN -- timer enable bit

0 = disable timer; this can be used to save power consumption
1 = allows timer to function normally

TSWAI -- timer stops while in wait mode bit

0 = allows timer to continue running during wait mode
1 = disables timer when MCU is in wait mode

TSFRZ -- timer and modulus counter stop while in freeze mode

0 = allows timer and modulus counter to continue running while in freeze mode
1 = disables timer and modulus counter when MCU is in freeze mode

TFFCA -- timer fast flag clear all bit

0 = allows timer flag clearing to function normally
1 = For TFLG1, a read from an input capture or a write to the output compare channel causes the corresponding channel flag, CnF, to be cleared. For TFLG2, any access to the TCNT register clears the TOF flag. Any access to the PACN3 and PACN2 registers clears the PAOVF and PAIF flags in the PAFLG register. Any access to the PACN1 and PACN0 registers clears the PBOVF flag in the PBFLG register.

Figure 8.2 Timer system control register 1 (TSCR1)

Timer System Control Flag2 (TSCR2)

	7	6	5	4	3	2	1	0
	TOI	0	0	0	TCRE	PR2	PR1	PR0
value after reset	0	0	0	0	0	0	0	0

TOI -- timer overflow interrupt enable bit
0 = interrupt inhibited
1 = interrupt requested when TOF flag is set
TCRE -- timer counter reset enable bit
0 = counter reset inhibited and counter free runs
1 = counter reset by a successful output compare 7
If TC7 = $0000 and TCRE = 1, TCNT stays at $0000 continuously. If TC7 = $FFFF and TCRE = 1, TOF will never be set when TCNT rolls over from $FFFF to $0000.

Figure 8.3 Timer system control register 2 (TSCR2)

Table 8.1 Timer counter prescale factor

PR2	PR1	PR0	Prescale Factor
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

- Only bit 7 (TOF) of TFLG2 is implemented if Bit 7 will be set whenever TCNT overflows.

Next…

- Input Capture function
- Read Chapter 8.5-8.7