- Prev
  - Subroutines & D-Bug12 Functions

- Today
  - Basic Concepts of I/O
  - I/O Addressing
  - I/O Synchronization
Overview of HCS12 Parallel Ports (1/3)

- The HCS12 members have from 48 to 144 I/O pins arranged in 3 to 12 ports.
- In general, a 68HCS12 I/O port has
  - I/O pins
  - a data register
  - A data direction register: set a bit to 1 (0) will configure the corresponding pin for output (input).
- All I/O pins serve multiple functions.
- When a peripheral function is enabled, its associated pins cannot be used as I/O pins.
- Each I/O port has several registers to support its operation.
- Registers related to I/O ports have been assigned a mnemonic name and the user can use these names to refer to them:
  ```
  movb #$FF,PTA ; output $FF to Port A
  ```
All I/O ports (except PAD0 and PAD1) have an associated data direction register and a data register.

The name of the data direction register is formed by adding the letters “DDR” as the prefix to the port name. For example, DDRA, DDRB, and DDRT.

To configure a pin for output, write a ‘1’ to the associated bit in the data direction register.

To configure a pin for input, write a ‘0’ to the associated bit in the data direction register.

```assembly
movb #$FF,DDRA ; configure port A for output
movb #0,DDRA ; configure port A for input
bset DDRA,$81 ; configure Port A pin 7 and 1 for output
```
The name of port data register is formed by adding letters “PT” as the prefix to the port name. For example, PTA, PTB, PTP, and PTT.

We can also use “PORT” as the prefix to the port name for port A, B, E, and K.

Output a value to a port is done by storing that value to the port data register.

```
  movb  #$FF,DDRH ; configure Port H for output
  movb  #$37,PTH   ; output the hex value 37 to port H
```

Input a value from an input port is done by loading from the port data register.

```
  movb  #0,DDRH    ; configure Port H for input
  ldaa  PTH        ; read data from port H into A
```

An I/O port may have up to eight associated registers.
Figure 1-1 MC9S12DP256B Block Diagram
Port A and Port B

- In expanded mode, Port A carries the time-multiplexed higher address/data signals A15/D15…A8/D8.
- In expanded mode, Port B carries the time-multiplexed lower address/data signals A7/D7…A0/D0.
- In single chip mode, these two ports are used as general I/O ports.
Port E

- Port E pins are used for bus control and interrupt service request signals.
- When a Port E pin is not used as control or interrupt signal, it can be used as general I/O pin.

Figure 7.5 Port E pins and their alternate functions
Port E Registers

- Port E assignment register (PEAR)
  - In expanded mode, the PEAR register assigns the function of each port E pin.
- MODE register
  - This register establishes the operation mode and other miscellaneous functions.
- Pull-up control register (PUCR)
  - This register selects the pull-up resistors for the pins associated with the core ports.
  - Port A, B, E, and K are in the core part.
- Reduced drive register (RDRIV)
  - This register selects reduced drive for the pins associated with the core ports.
  - This gives reduced power consumption
- External bus interface control register (EBICTL)
  - Only bit 0 is implemented (ESTR).
  - The ESTR bit enables/disables the E clock stretching.
RDPK: reduced drive of Port K
0 = All Port K pins have full drive enabled
1 = All Port K pins have reduced drive enabled
RDPE: reduced drive of Port E
0 = All Port E pins have full drive enabled
1 = All Port E pins have reduced drive enabled
RDPB: reduced drive of Port B
0 = All Port B pins have full drive enabled
1 = All Port B pins have reduced drive enabled
RDPA: reduced drive of Port A
0 = All Port A pins have full drive enabled
1 = All Port A pins have reduced drive enabled

Figure 7.9 Reduced Drive Register (RDRIV)

PUPKE: pull-up Port K enable
0 = Port K pull-up resistors are disabled
1 = Port K pull-up resistors are enabled
PUPEE: pull-up Port E enable
0 = Port E input pins 7 and 4-0, pull-up resistors are disabled
1 = Port E input pins 7 and 4-0, pull-up resistors are enabled
PUPBE: pull-up Port B enable
0 = Port B pull-up resistors are disabled
1 = Port B pull-up resistors are enabled
PUPAE: pull-up Port A enable
0 = Port A pull-up resistors are disabled
1 = Port A pull-up resistors are enabled

Figure 7.8 Pull-Up control register
Port T

- Has Port T data register (PTT), Port T data direction register (DDRT), Port input register (PTIT), reduced drive register (RDRT), pull device enable register (PERT), and port polarity select register (PPST)
  - The PTIT register allows the user to read back the status of Port T pins.
  - The RDRT register can configure the drive strength (current output) of each port pin as either full or reduced load.
  - The PERT register is used to enable an input Port T pin pull-up or pull-down device.
  - The PPST register selects whether a pull-down or pull-down device is connected to the pin.
- Port T pins are also used as timer input capture/output compare pin.
RDRT[7:0]: Reduced drive Port T
0 = full drive strength at output
1 = associated pin drives at about 1/3 of the full drive strength

Figure 7.11 Port T Reduced Drive register (RDRT)

PERT[7:0]: pull device enable Port T
0 = pull-up or pull-down is disabled
1 = either pull-up or pull-down is enabled

Figure 7.12 Port T Pull Device Enable register (PERT)

PPST[7:0]: pull device enable Port T
0 = A pull-up device is connected to the associated port T pin, if enabled
   by the associated bit in register PERT and if the port is used as input or as wired-or output
1 = A pull-down device is connected to the associated Port T pin, if enabled
   by the associated bit in register PERT and if the port is used as input

Figure 7.13 Port T Polarity Select register (PPST)
Port S & Port M

- Port S pins are used as general I/O, serial communication interface, and serial peripheral interface pins.

- Port M has all the equivalent registers that Port S has and also a module routing register (MODRR).
Port H, J, and P

- These three I/O ports have the same set of registers:
  - Port I/O register (PTH, PTJ, PTP)
  - Port Input Register (PTIH, PTIJ, PTIP)
  - Port Data Direction Register (DDRH, DDRJ, DDRP)
  - Port Reduced Drive Register (RDRH, RDRJ, RDRP)
  - Port Pull Device Enable Register (PERH, PERJ, PERP)
  - Port Polarity Select Register (PPSH, PPSJ, PPSP)
  - Port Interrupt Enable Register (PIEH, PIEJ, PIEP)
  - Port Interrupt Flag Register (PIFH, PIFJ, PIFP)

- These ports have edge-triggered interrupt capability in the wired-OR fashion.

- The SPI function pins can be rerouted to Port H and P.

- The interrupt edges can be rising or falling and are programmed through Port Device Enable Register and Port Polarity Select Register.

- The Port Interrupt Register allows the user to enable interrupts on these three ports.
Figure 7.19 Port H Interrupt Enable Register (PIEH)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIEH7</td>
<td>PIEH6</td>
<td>PIEH5</td>
<td>PIEH4</td>
<td>PIEH3</td>
<td>PIEH2</td>
<td>PIEH1</td>
<td>PIEH0</td>
</tr>
</tbody>
</table>

reset: 0 0 0 0 0 0 0 0

PIEH[7:0]: Interrupt enable Port H
0 = interrupt is disabled
1 = interrupt is enabled

Figure 7.20 Port P Interrupt Flag Register (PIFH)

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIFH7</td>
<td>PIFH6</td>
<td>PIFH5</td>
<td>PIFH4</td>
<td>PIFH3</td>
<td>PIFH2</td>
<td>PIFH1</td>
<td>PIFH0</td>
</tr>
</tbody>
</table>

reset: 0 0 0 0 0 0 0 0

PIFH[7:0]: Interrupt flag Port H
0 = no active edge pending
1 = active edge has occurred (writing a '1' clears the associated flag)
Figure 7.21 Port H pins and their alternate functions

Figure 7.22 Port J pins and their alternate functions

Figure 7.23 Port P pins and their alternate functions
Port AD0 and AD1

- Many HCS12 devices have two 8-channel A/D converters (AD0 and AD1).
- Device that has only one 8-channel module is referred to as AD.
- When A/D functions are disabled, these two ports can be used as general input port.
- These two ports do not have data direction registers.
- Each module has a Digital Input Enable Register. In order to use an A/D pin as a digital input, one needs to set its associated bit in this register.

```
<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEN7</td>
<td>IEN6</td>
<td>IEN5</td>
<td>IEN4</td>
<td>IEN3</td>
<td>IEN2</td>
<td>IEN1</td>
<td>IEN0</td>
</tr>
</tbody>
</table>
```

reset: 0 0 0 0 0 0 0 0

IENx: ATD digital input enable on channel x
0 = disable digital input buffer to PTADx pin
1 = enable digital input buffer to PTADx pin

Figure 7.24 ATD Input enable register (ATD0DIEN and ATD1DIEN)
Next...

- Interfacing with I/O devices
- Read Chapter 7.1-7.6